In the claims: The claims are as follows.

1. (Original) A semiconductor component (30) having a silicon-bearing layer (32) and a praseodymium oxide layer (40), characterized in that arranged between the silicon-bearing layer (32) and the praseodymium oxide layer (40) is a mixed oxide layer (34) containing silicon, praseodymium and oxygen, which is of a layer thickness of less than 5 nanometers.

2. (Original) A semiconductor component as set forth in claim 1 wherein the mixed oxide layer (34) is of a layer thickness of a maximum of 3 nanometers.

3. (Previously presented) A semiconductor component as set forth in claim 1 wherein the mixed oxide (34) is a pseudo-binary, non-stoichiometric silicate or an alloy of the type $(Pr_2O_3)_x(SiO_2)_{1-x}$.

4. (Currently amended) A semiconductor component as set forth in claim 3, wherein the mixed oxide (34) is an alloy of the type $(Pr_2O_3)_x(SiO_2)_{1-x}$, and ~~—~~wherein x increases from a first value at an interface of the mixed oxide layer with ~~between —~~the silicon-bearing layer (32) to a second value at an interface of the mixed oxide layer with~~and~~ the praseodymium oxide layer (40).

The mixed oxide layer is a $(Pr_2O_3)_x(SiO_2)_{1-x}$ layer wherein the coefficient x at the interface 36 is of a value 0.3 and at an interface 38 to an adjacent praseodymium oxide layer (Pr_2O_3) 40 it is of a value 1.

5. (Previously presented) A semiconductor component as set forth in claim 1 wherein the silicon-bearing layer (32) comprises doped or undoped silicon-germanium.

6. (Previously presented) A semiconductor component as set forth in

claim 1 wherein the silicon-bearing layer comprises doped or undoped silicon.

7. (Previously presented) A semiconductor component 30 as set forth in claim 5 wherein the silicon-germanium layer or the silicon layer has an (001) orientation at the interface to the mixed oxide layer.

8. (Previously presented) An MOSFET as set forth in claim 1.

9. (Previously presented) A memory cell as set forth in claim 1.

10. (Previously presented) A production process for an electronic component with a step of depositing a praseodymium oxide layer (40) on a silicon-bearing layer (32), characterized in that prior to said deposit step a step of depositing a mixed oxide layer (34) containing silicon, praseodymium and oxygen.

11. (Original) A process as set forth in claim 10 wherein the steps of depositing a mixed oxide layer (34) and depositing a praseodymium oxide layer (40) are effected in the form of deposition out of the gaseous phase.

12. (Original) A process as set forth in claim 11 wherein the deposit steps are effected by means of molecular beam deposition.

13. (Original) A process as set forth in claim 11 wherein the deposit steps are effected by means of chemical vapor phase deposition.

14. (Previously presented) A process as set forth in claim 10 wherein the step of depositing the mixed oxide layer (34) is effected in an oxygen-bearing gas atmosphere.

15. (Previously presented) A process as set forth in claim 10

wherein the step of depositing the praseodymium oxide layer (40) is effected in an oxygen-bearing gas atmosphere.

16. (Previously presented) A process as set forth in claim 10 wherein the step of depositing the mixed oxide layer (34) is effected by means of a starting material which contains or consists of praseodymium oxide in the form Pr_6O_{11}.

17. (Previously presented) A process as set forth in claim 10 wherein the step of depositing the praseodymium oxide layer (40) is effected by means of a starting material containing praseodymium oxide in the form Pr_6O_{11}.

18. (Previously presented) A process as set forth in claim 10 wherein the step of depositing the mixed oxide layer (34) is effected at a temperature of a maximum of 680°C.

19. (Previously presented) A process as set forth in claim 12 wherein the step of depositing the mixed oxide layer (34) is effected at a temperature of between 600°C and 650°C.

20. (Previously presented) A process as in claim 10, wherein the step of depositing a mixed oxide layer (34) containing silicon, praseodymium and oxygen is effected at a substrate temperature of less than 700°C.

21. (Previously presented) A process as in claim 20, wherein the mixed oxide layer (34) containing silicon, praseodymium and oxygen, is deposited to a layer thickness of less than 5 nanometers.